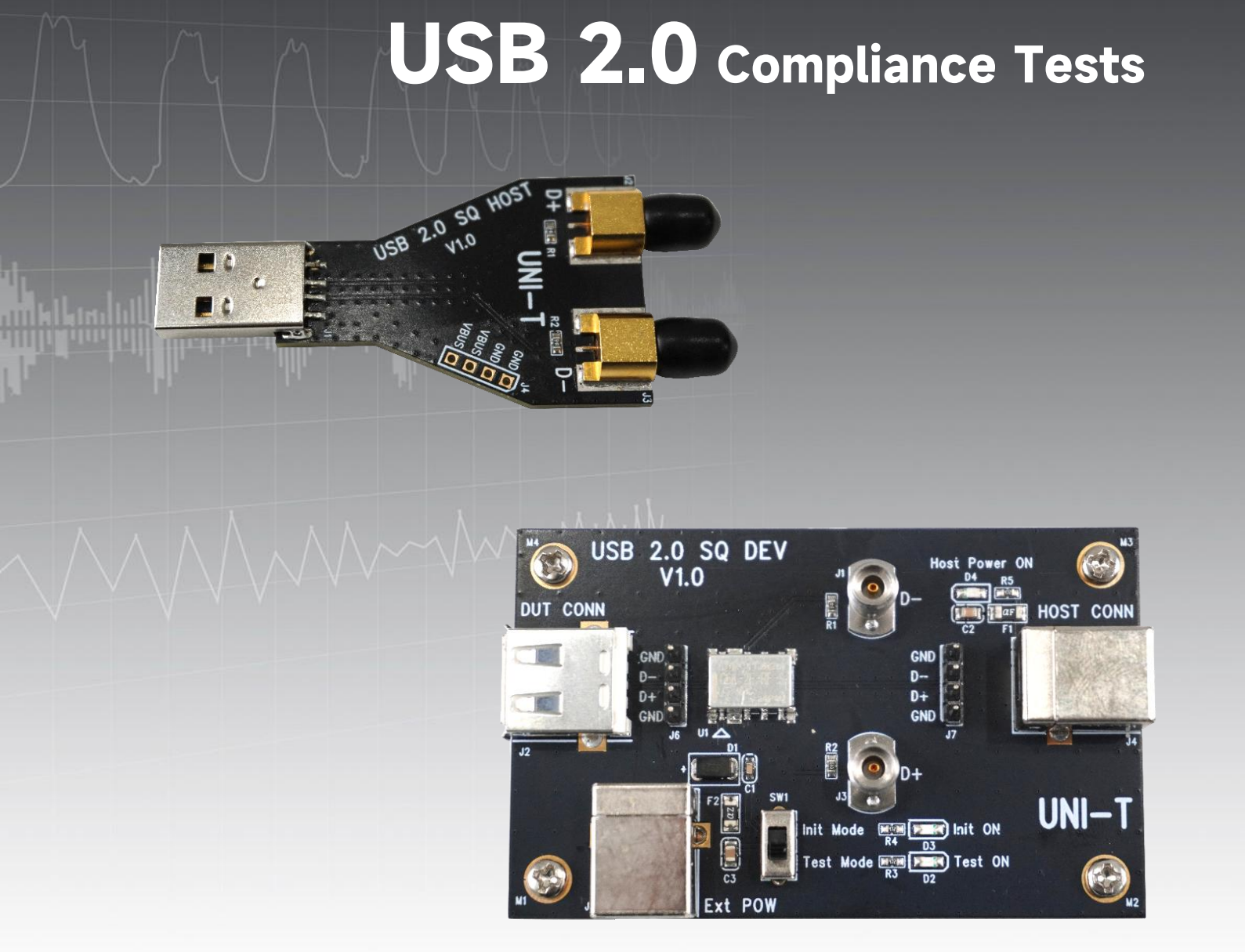


USB 2.0 Compliance Tests

The image displays two black printed circuit boards (PCBs) used for USB 2.0 compliance testing, both branded with the UNI-T logo.

The top PCB is labeled "USB 2.0 SQ HOST V1.0". It features a standard USB-A male connector on the left. On the right, it has two gold-plated BNC connectors labeled "D+" and "D-". A small header on the bottom left is labeled "GND", "VBI", and "VREF".

The bottom PCB is labeled "USB 2.0 SQ DEV V1.0". It features a USB-A female connector on the left, labeled "DUT CONN". On the right, it has two gold-plated BNC connectors labeled "D-" and "D+", and a large rectangular connector labeled "HOST CONN". The board includes various components such as resistors (R1, R2, R3, R4), capacitors (C1, C2, C3), a switch (SW1), and a power jack (J1) labeled "Ext POW". It also has four mounting holes labeled M1, M2, M3, and M4. The board is populated with several surface-mount components and a small integrated circuit (U1).



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USB 2.0 Compliance Analysis Overview

USB (Universal Serial Bus) 2.0 is a mature external connection standard. Its plug-and-play design eliminates complex disassembly/assembly of computer boards, offering advantages like ease of use, functional flexibility, and efficient transmission.

For USB 2.0 designers, thorough compliance testing is mandatory before product launch to ensure adherence to industry standards. Only certified devices are permitted to display the USB-IF logo. Key tests include eye diagram analysis and parametric checks for low-speed, full-speed, and high-speed devices/hubs.

Test Items

- Signal quality tests
- Non-signal quality tests
- Power tests (not supported)

Test Item	Sub-items (Device)	Sub-items (Host)	Sub-items (Hub)
High-Speed Signal Quality	Eye Diagram	Eye Diagram	Eye Diagram
	End-of-Packet Width	End-of-Packet Width	End-of-Packet Width
	Signal Rate	Signal Rate	Signal Rate
	Edge Monotonicity	Edge Monotonicity	Edge Monotonicity
	Consecutive Jitter	Consecutive Jitter	Consecutive Jitter
	JK Paired Jitter	JK Paired Jitter	JK Paired Jitter
	KJ Paired Jitter	KJ Paired Jitter	KJ Paired Jitter
	Edge Rise Rate	Edge Rise Rate	Edge Rise Rate
	Edge Fall Rate	Edge Fall Rate	Edge Fall Rate
	Rise Time	Rise Time	Rise Time
	Fall Time	Fall Time	Fall Time
High-Speed Non-Signal Quality	Chirp Timing Test EL28_EL29_EL31	Chirp Test EL33_EL34	
	Suspend Test	Chirp Test EL35	
	Resume Test	Suspend Test	
	High-Speed Reset	Resume Test	
	Suspend Reset	Packet Parameter Test EL21_EL23_EL25	
	Packet Parameter Test EL21_EL22_EL25	Packet Parameter Test EL55	
	Packet Parameter Test EL22	Packet Parameter Test EL22	
	Receiver Sensitivity EL16_EL17	Undriven J Voltage EL8	
	Receiver Sensitivity EL18	Undriven K Voltage EL8	
	Undriven J Voltage EL8	SE0 State Voltage EL9	
	Undriven K Voltage EL8		
	SE0 State Voltage EL9		
Power Test	Inrush Current	V _{bus} Voltage Drop	
	Backplane Current	V _{bus} Voltage Sag	

3 Test Equipment

3.1 Requirements

- Oscilloscope: \geq bandwidth 2GHz, sample rate \geq 5GSa/s, with USB 2.0 compliance software.
- USB 2.0 Compliance Test Fixture: provides signal access points.
- Active Differential Probe and Active Single-ended Probe: \geq bandwidth 2GHz.
- Packet Generation Software: [HSETT] or [XHSETT] (USB-IF official).

3.2 Configuration

Oscilloscope	\geq 2GHz bandwidth, recommended: MSO7000X, MSO8000HD series
Active Differential Probe	\geq 2GHz, recommended: UT-PD2500
Active Single-ended Probe	\geq 2GHz, recommended: UT-PA2000 (\geq 2 sets)
Test Fixture	UNI-T USB 2.0 Test Fixture (USB20-SQ-HD) or association-recommended
USB Compliance Analysis Software	UNI-T CTS-USB20
USB-IF Packet Generation Software	Official Association Packet Generation Software [HSETT] or [XHSETT]

3.3 Equipment Introduction

Oscilloscopes:

UNI-T's high-bandwidth oscilloscopes, MSO8000HD and MSO7000X series, offer bandwidths from 1GHz to 8GHz and sampling rates up to 20GSa/s. MSO8000HD's 12-bit ADC provides accurate measurement data essential for compliance testing. Its excellent signal integrity characteristics, such as noise floor below 800 μ V at 50mV/div, ENOB >7bits across full bandwidth, and low intrinsic jitter of 150fs RMS, ensure reliable compliance analysis data. MSO7000X series offers a cost-effective testing solution.



MSO8804HD | 8GHz | 20GSa/s | 55ps

MSO8504HD | 5GHz | 20GSa/s | 88ps



MSO7000X | 2GHz | 10GSa/s | 175ps

Active Probes:

The association requires probes with a bandwidth of at least 1.5GHz for compliance analysis to ensure accurate results. UNI-T offers self-developed UT-PD2500 (2.5GHz) active differential probes, and UT-PA2000 (2GHz) active single-ended probes to support USB 2.0 compliance testing. These probes provide reliable DUT connection.



UT-PD2500 | 2.5GHz | 150ps



UT-PA2000 | 2GHz | 175ps

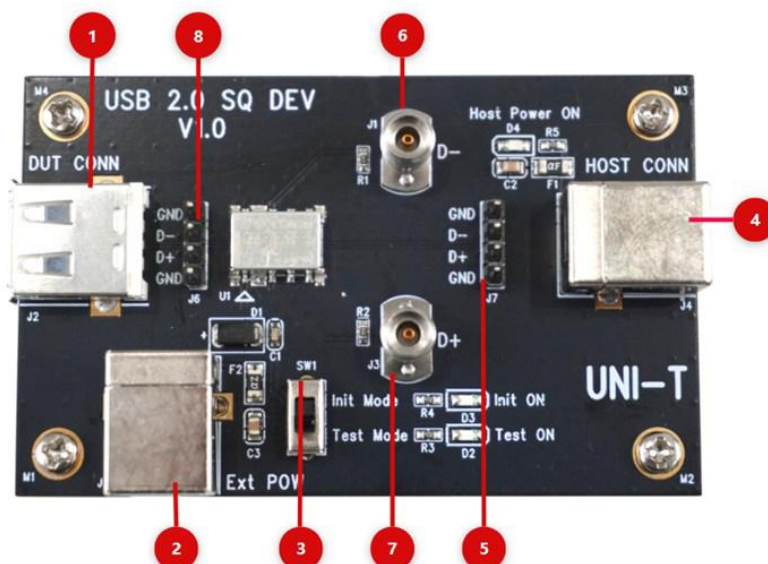
Test Fixture:

USB 2.0 test fixture consists of a Host test fixture (bottom left), a Device test fixture (top left), a communication USB 2.0 cable (10cm), and a power supply USB 2.0 cable (20cm). This fixture supports all High-Speed/Full-Speed/Low-Speed signal quality tests and all signal/non-signal quality tests except receiver sensitivity. Power tests are not supported with this fixture.



UT-USB20-SQ-HD

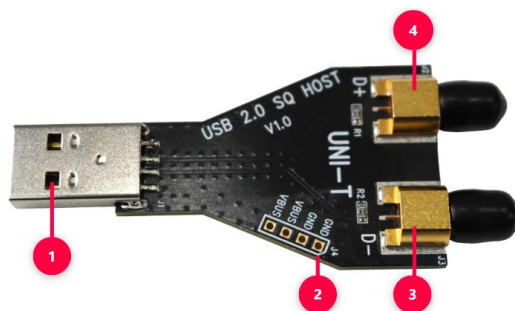
Fixture Layout Introduction



High-Speed Device Signal Quality Test Fixture

No.	Interface	Description
1	DUT CONN	DUT Connection Port, USB-A Female
2	EXT POW	Fixture Power Supply Interface, USB-B Female
3	SW1	Test Mode Switch: Toggles between Init mode and Test mode
4	HOST CONN	Host Connection Interface (connects to PC running test software), USB-B Female
5	J7	USB 2.0 Far-End Test Point
6	J1	USB Signal Differential Negative Voltage Output (connect to scope via SMA)
7	J3	USB Signal Differential Positive Voltage Output (connect to scope via SMA)
8	J6	USB 2.0 Near-End Test Point

High-Speed Host Signal Quality Test Fixture



No.	Interface	Description
1	J1	Connects to PC running test software (acting as Host), USB-A Male
2	J4	V _{BUS} Voltage Test Point (use single-ended probe)
3	J3	USB Signal Differential Negative Voltage Output (connect to scope via SMA)
4	J2	USB Signal Differential Positive Voltage Output (connect to scope via SMA)

Packet Generation Software:

[HSETT] and **[XHSETT]** are USB signal packet generation software provided by the USB-IF Association.

For more information: <https://www.usb.org/document-library/xhsett>

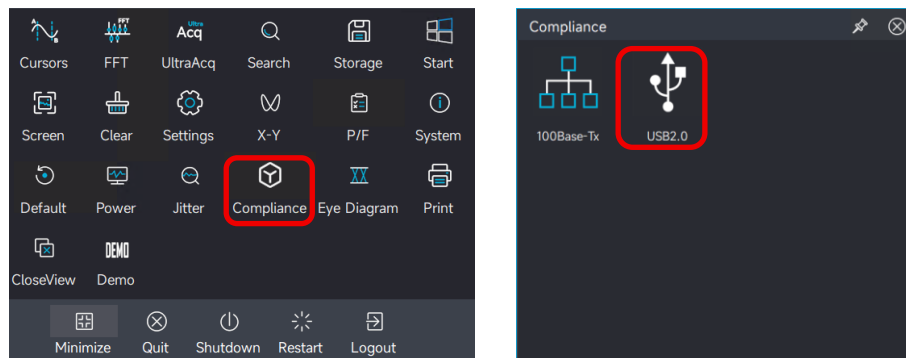
For configuration details: Refer to *"USB 2.0 Signal Quality Test Fixture User Manual REV.1.0"*

Compliance Analysis Software:

CTS-USB20 is UNI-T's USB 2.0 compliance analysis software. It automates all compliance tests through scripting, significantly reducing execution time to within minutes. The software features automatic pass/fail determination, parameter editing, and report generation. Simple setup allows users to complete compliance analysis and generate comprehensive reports within minutes, minimizing user intervention.

- Allows users to execute single or multiple tests.
- Highly optimized, intuitive user interface visualizing oscilloscope and DUT connections for rapid test configuration and electrical performance validation.
- Fully automated oscilloscope testing process, auto-setting parameters for each test item.
- Detailed test reports with Pass/Fail results, data tables, and waveform images.
- Configurable test parameters and traces for debugging and characterization.
- Supports multiple test runs for result verification.

Click the compliance icon in the Start Menu to launch the compliance test function, as shown below:



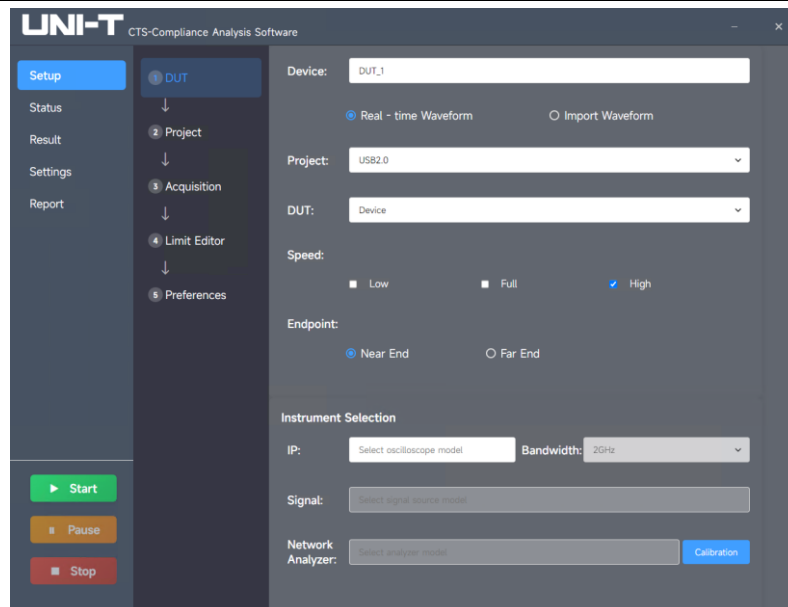
Launching Compliance Analysis Software

Test Setup

DUT:

Supports: Device, Host, Hub. Select other options as needed.

Note: If testing locally, oscilloscope model selection is not required.



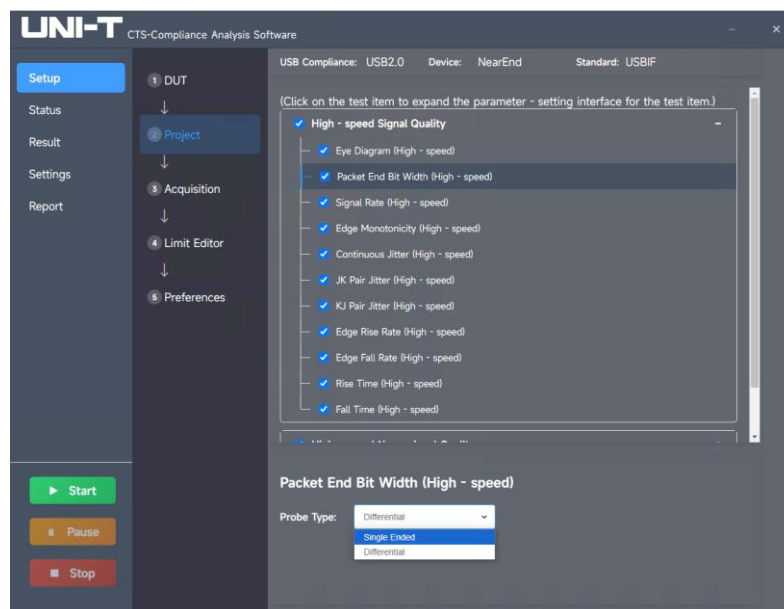
DUT Settings

Test Items:

Supports: Low-Speed Signal Quality, Full-Speed Signal Quality, High-Speed Signal Quality, High-Speed Non-Signal Quality, Power Tests (Currently Unsupported).

Note: Available test items vary depending on the selected DUT type.

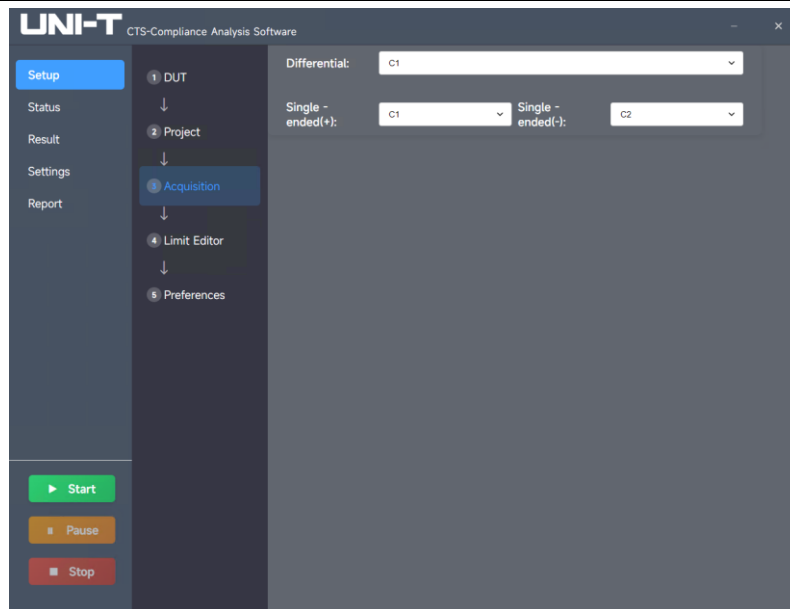
Click + or - to expand/collapse measurement sub-items. After expanding, select individual sub-items as needed by clicking the checkbox ☐. Selected sub-items can be configured individually, such as selecting the corresponding probe type based on the signal type for each measurement.



Test Item Settings

Waveform Acquisition:

Select the analog input channel(s) for differential/single-ended probes based on specific test requirements.



Waveform Acquisition Settings

Limits Editor:

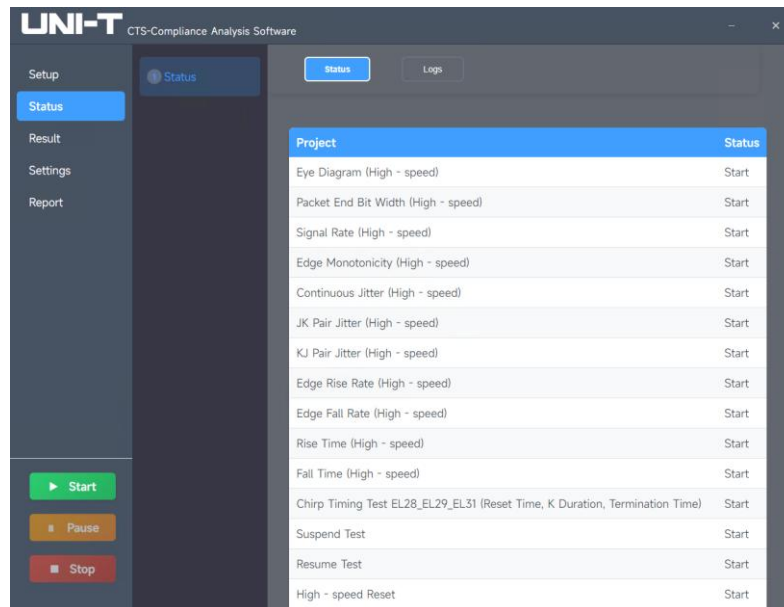
For selected test items, users can view the compliance standards in the Limit Editor, which can also customize the limits according to their requirements.

Item	Unit	Lower Comparison	Lower	Upper Comparison	Upper
Eye Diagram (High - speed)	Hits	>=	0	<=	0
Packet End Bit Width (High - speed)	bits	>=	7.5	<=	8.5
Signal Rate (High - speed)	Mbps	>=	479.76	<=	480.24
Edge Monotonicity (High - speed)	mV	N.A.	N.A.	<=	50
Maximum Continuous Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Minimum Continuous Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Root Mean Square Continuous Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Maximum JK Pair Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Minimum JK Pair Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Root Mean Square JK Pair Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Maximum KJ Pair Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Minimum KJ Pair Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Root Mean Square KJ Pair Jitter (High - speed)	ps	N.A.	N.A.	N.A.	N.A.
Edge Rise Rate (High - speed)	V/us	N.A.	N.A.	<=	2133

Limits Editor Interface

Test Status:

The Test Status interface shows the status (Pending, In Progress, Completed, Skipped) of selected test items. The Log interface displays the test log (status descriptions with timestamps, e.g., Test Started, Skipped, Completed, Timeout, Paused) after testing.



Test Status Interface

Test Result:

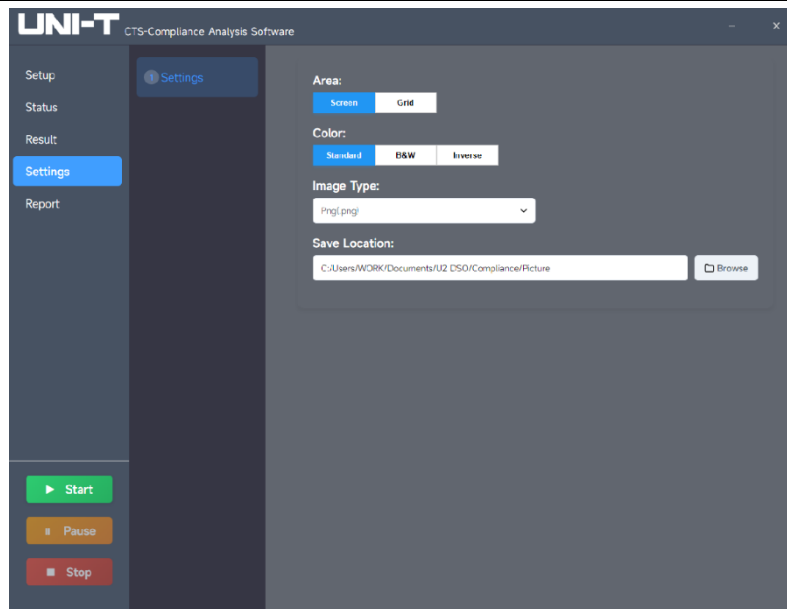
After testing, view results for executed test items in the Test Results interface. The results table includes: Name, Speed, Lower Limit, Upper Limit, Unit, Measured Value, Margin, Description, and Result.

Item	Name	Speed	Lower	Upper	Unit	Test Item	Marg
Eye Diagram (High - speed)	Eye Diagram (High - speed)	High Speed	N.A.	0.000	hits	0	High
Packet End Bit Width (High - speed)	Packet End Bit Width (High - speed)	High Speed	7.500	8.500	bits	7943	High
Signal Rate (High - speed)	Signal Rate (High - speed)	High Speed	479.760	480.240	Mbps	480.001	High
Edge Monotonicity (High - speed)	Edge Monotonicity (High - speed)	High Speed	N.A.	50.000	mV	0.000	High
Continuous Jitter (High - speed)	Maximum Continuous Jitter (High - speed)	High Speed	N.A.	N.A.	ps	46.238	N.A.
Continuous Jitter (High - speed)	Minimum Continuous Jitter (High - speed)	High Speed	N.A.	N.A.	ps	-54.748	N.A.
Continuous Jitter (High - speed)	Root Mean Square Continuous Jitter (High - speed)	High Speed	N.A.	N.A.	ps	13.699	N.A.

Test Results Interface

Save Settings:

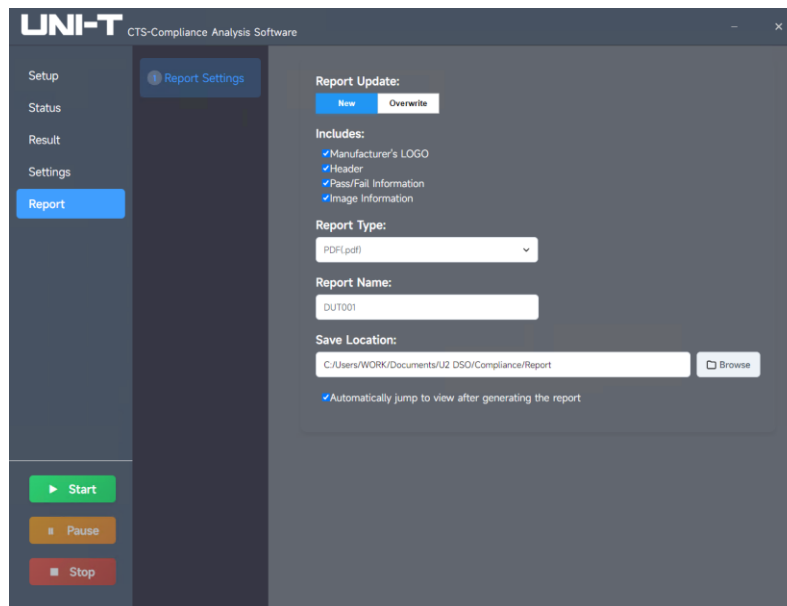
Click Save Settings. In the pop-up window, configure screenshot capture settings: Capture Area (Screen, Grid), Screenshot Color (Standard, B&W, Inverted), Image Type (.png/.bmp/.tiff/.gif/.jpeg), Save Location (customizable).



Save Settings Interface

Test Report:

Click Test Report to open the Report Settings window. Configure report details: Report Update, Report Contents, Report Type, Report Name, Save Location, and options for auto-incrementing report names, auto-creating reports, auto-opening reports, etc.



Test Report Settings Interface

USB2.0 Compliance Test Report

Overall Information

Application Info	
Application Name	CTS USB
Application Version	1.0.0
Device Info	
Scope Model Number	MSO7000X
Scope Software Version	3.01.0000
Scope Serial Number	<AMX7224230045>
Test Info	
DUT ID	DUT_1
Overall Test Result	Pass
Compliance Limits	USB 2.0 Specification
Test Time	2025-07-16 10:04:41.002
Excute Time	00:08:53.878
Acquisition Mode	Live
Suite	Device

Result Summary

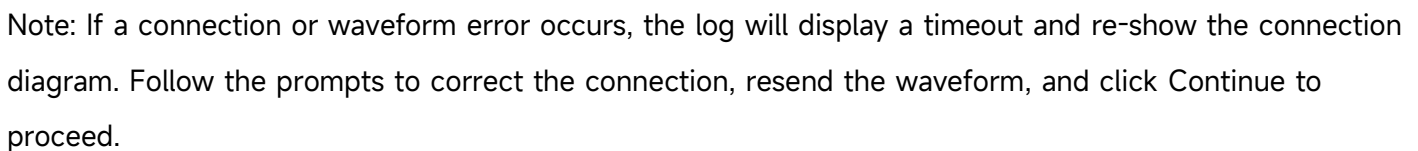
Test Name	Result	Measure Value	Pass Limit
Eye Diagram	Pass	0nits	Value<=0.000
Consecutive Jitter	Pass	33.676ps	N.A.
		-51.601ps	N.A.
		12.286ps	N.A.
Paired JK Jitter	Pass	25.516ps	N.A.
		-29.493ps	N.A.
		9.799ps	N.A.
Paired KJ Jitter	Pass	34.656ps	N.A.
		-43.777ps	N.A.
		16.178ps	N.A.
EOP Width	Pass	7.930bits	7.500<=Value<=8.500
Signalling Rate	Pass	479.948Mbps	479.760<=Value<=480.240
Edge Monotonicity	Pass	0.000mV	Value<=50.000
Rise Time	Pass	633.578ps	Value<=300.000
Fall Time	Pass	635.780ps	Value<=300.000
Rising Edge Rate	Pass	943.917V/us	Value<=2133.000
Falling Edge Rate	Pass	940.685V/us	Value<=2133.000
EL28_EL29_EL31(Reset time, K Duration, Termination Time)	Pass	107.150us	2.500<=Value<=6000.000
		1.302ms	1.000<=Value<=7.000
		0.328us	Value<=500.000
Suspend	Pass	3.000ms	3.000<=Value<=3.125
Resume	Pass	0.107ms	Value<=3.000
		3.199ms	3.100<=Value<=6.000
		1.251ms	1.000<=Value<=7.000
Reset From HS	Pass	0.360us	Value<=500.000
		1007.549us	2.500<=Value<=6000.000
		1.250ms	1.000<=Value<=7.000
Reset From Suspend	Pass	0.157us	Value<=500.000

After testing, a comprehensive report is generated immediately, including Pass/Fail results, data tables, and screenshots for each test.

4.1 Signal Quality Tests

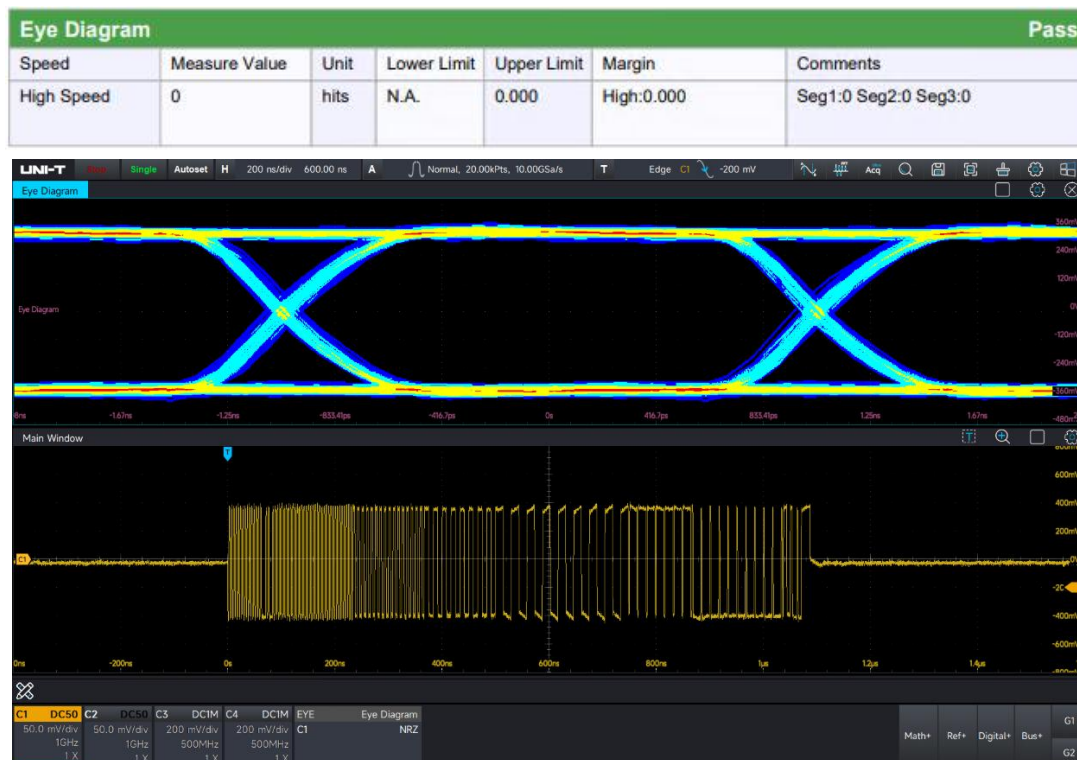
USB 2.0 signal eye diagram test results must comply with the standard eye diagram template provided by the USB-IF association. In USB 2.0 compliance testing, the eye diagram is a key reference, revealing most aspects of signal integrity, including jitter and rise speed. Therefore, this test should be performed multiple times to ensure accuracy. The eye diagram test automatically plots the eye and compares it to the standard template, providing a direct test result.

- (1) Open the compliance software: In **Test Setup** —> **Test Items**, click + to expand sub-items, select **Eye Diagram**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Set up the test environment according to the connection diagram prompted by the software. After confirmation, click **Continue** to start the test.



- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode. After completing the operations, click **Continue**.

- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms. eform images.



Eye Diagram Test Results

4.1.2 End-of-Packet Width

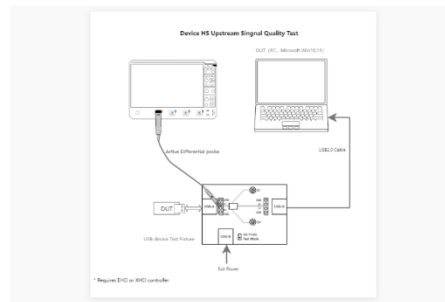
All USB packets end with an End-of-Packet (EOP) domain. The EOP width is defined in bit times. The EOP width for a Start-of-Frame (SOF) packet must be between 39.5bits and 40.5bits. For non-SOF packets, the EOP width must be between 7.5bits and 8.5bits.

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **End-of-Packet Width**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

Device-HS-EOP Width

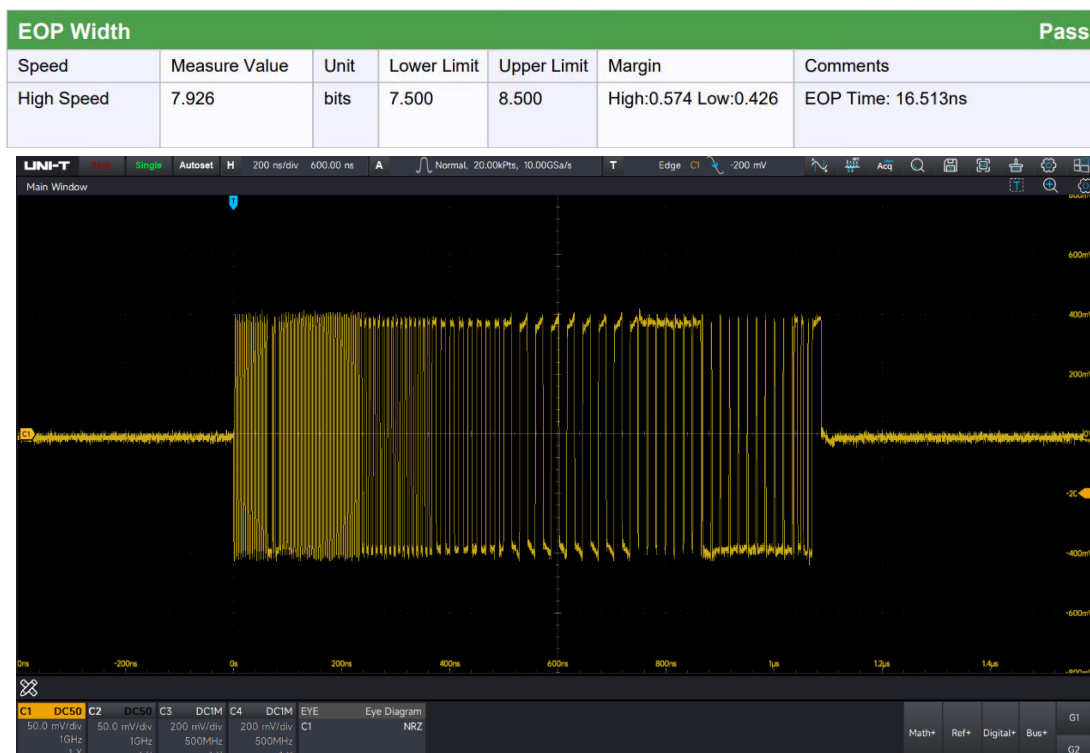
1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert a differential probe into the [D+ & D-] pins of the fixture [J6], and connect the other end to the oscilloscope according to the selected channel.



Continue Retry Skip

Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode. After completing the operations, click **Continue**.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.



End-of-Packet Width Test Results

4.1.3 Signal Rate

High-Speed Data Rate (THSDRAT): Nominal 480.00Mb/s, required accuracy $\pm 0.05\%$ (500ppm).

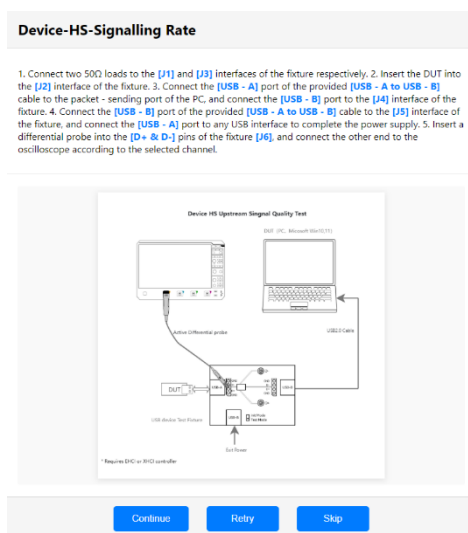
Full-Speed Data Rate (TFDRATE): Nominal 12.000Mb/s, required accuracy $\pm 0.25\%$ (2,500ppm).

Low-Speed Data Rate (TLDRATE): Nominal 1.50Mb/s, required accuracy $\pm 1.5\%$ (15,000ppm).

Test Procedure:

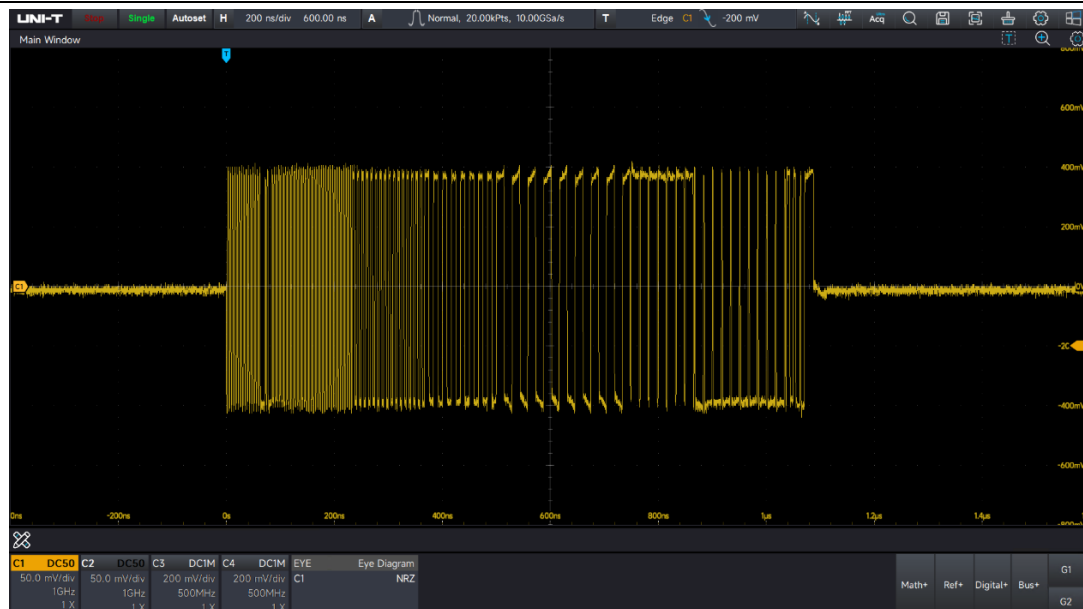
- (1) Open compliance software: **Test Setup** → **Test Items**, click **+**, select **Signal Rate**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.



- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. After the test is completed, a test report will be automatically generated, which includes test results, test waveform images, etc.

Signalling Rate						Pass
Speed	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments
High Speed	480.092	Mbps	479.760	480.240	High:0.148 Low:0.332	Test_Packet Signal Time: 1087.291 ns



Signal Rate Test Results

4.1.4 Edge Monotonicity

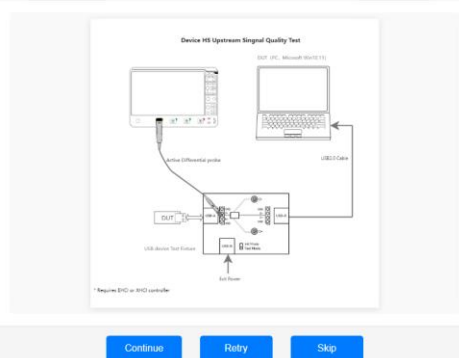
Edge monotonicity must be verified for every edge throughout each upstream/downstream data packet. For this test, as well as edge rise/fall time and edge rise/fall rate tests, special attention is required. To capture 500ps edge information, at least 10 sample points are needed on the edge, the system rise time should be controlled below 180ps, the sampling rate should be at least 10GSa/s, and the error percentage should be <10% for accurate testing.

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Edge Monotonicity**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

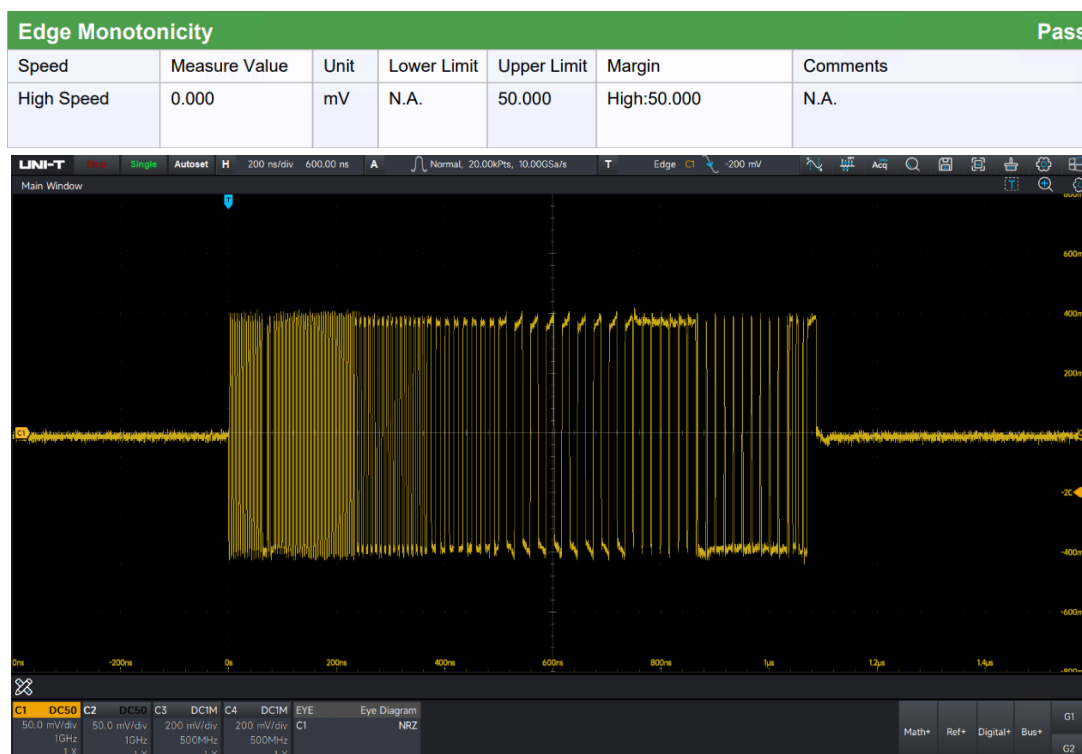
Device-HS-Edge Monotonicity

1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert a differential probe into the [D+ & D-] pins of the fixture [J6], and connect the other end to the oscilloscope according to the selected channel.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms. eform images.



Edge Monotonicity Test Results

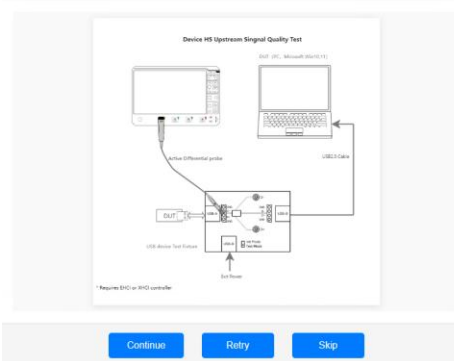
4.1.5 Consecutive Jitter

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Consecutive Jitter**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

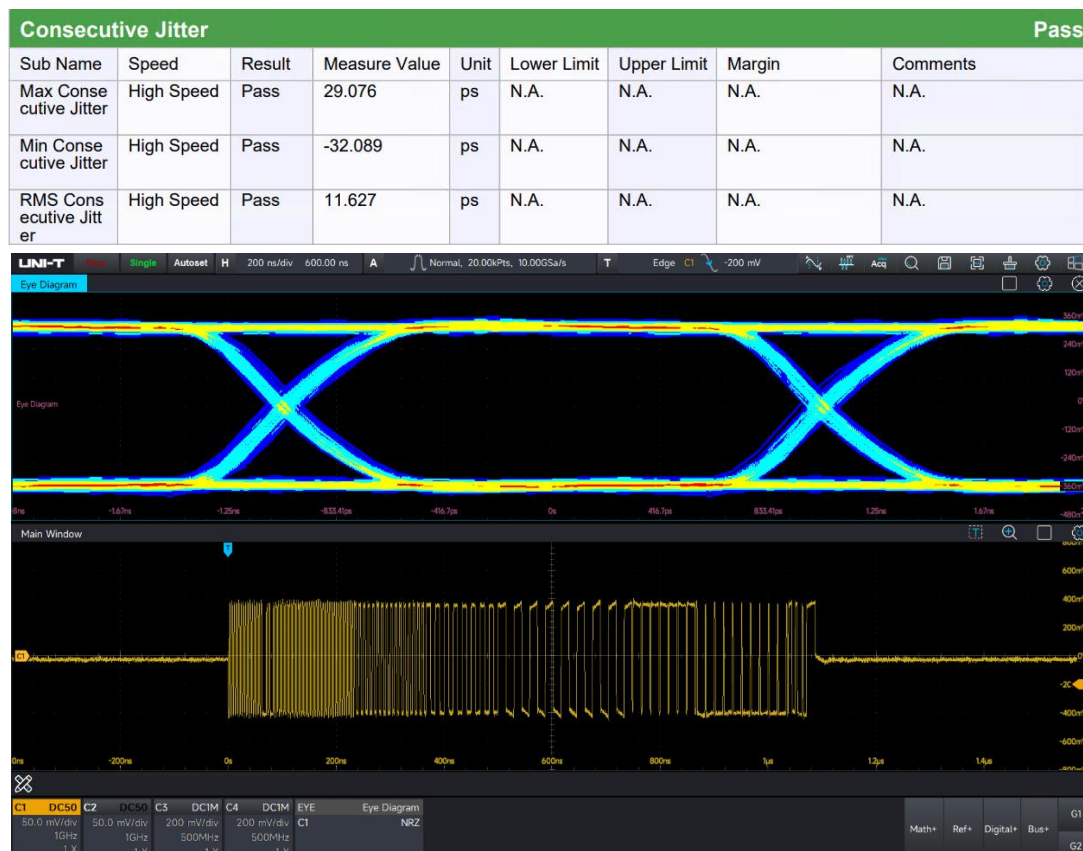
Device-HS-Consecutive Jitter

1. Connect two 50Ω loads to the **[J1]** and **[J3]** interfaces of the fixture respectively. 2. Insert the DUT into the **[J2]** interface of the fixture. 3. Connect the **[USB - A]** port of the provided **[USB - A to USB - B]** cable to the packet - sending port of the PC, and connect the **[USB - B]** port to the **[J4]** interface of the fixture. 4. Connect the **[USB - B]** port of the provided **[USB - A to USB - B]** cable to the **[J5]** interface of the fixture, and connect the **[USB - A]** port to any USB interface to complete the power supply. 5. Insert a differential probe into the **[D+ & D-]** pins of the fixture **[J6]**, and connect the other end to the oscilloscope according to the selected channel.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.

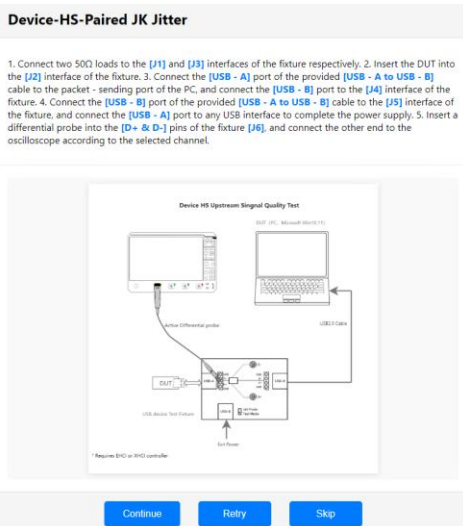


Consecutive Jitter Test Results

4.1.6 JK Pair Jitter

Test Procedure:

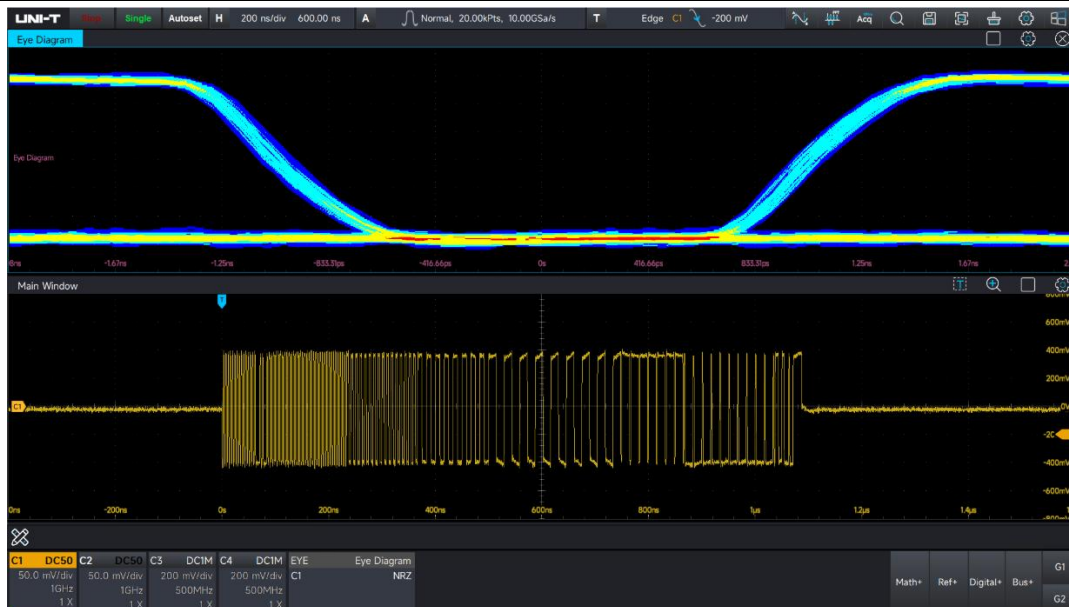
- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **JK Pair Jitter**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.

Paired JK Jitter								Pass
Sub Name	Speed	Result	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments
Max JK Jitter	High Speed	Pass	61.456	ps	N.A.	N.A.	N.A.	N.A.
Min JK Jitter	High Speed	Pass	-54.997	ps	N.A.	N.A.	N.A.	N.A.
RMS JK Jitter	High Speed	Pass	22.624	ps	N.A.	N.A.	N.A.	N.A.



JK Pair Jitter Test Results

4.1.7 KJ Pair Jitter

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **KJ Pair Jitter**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

Device-HS-Paired KJ Jitter

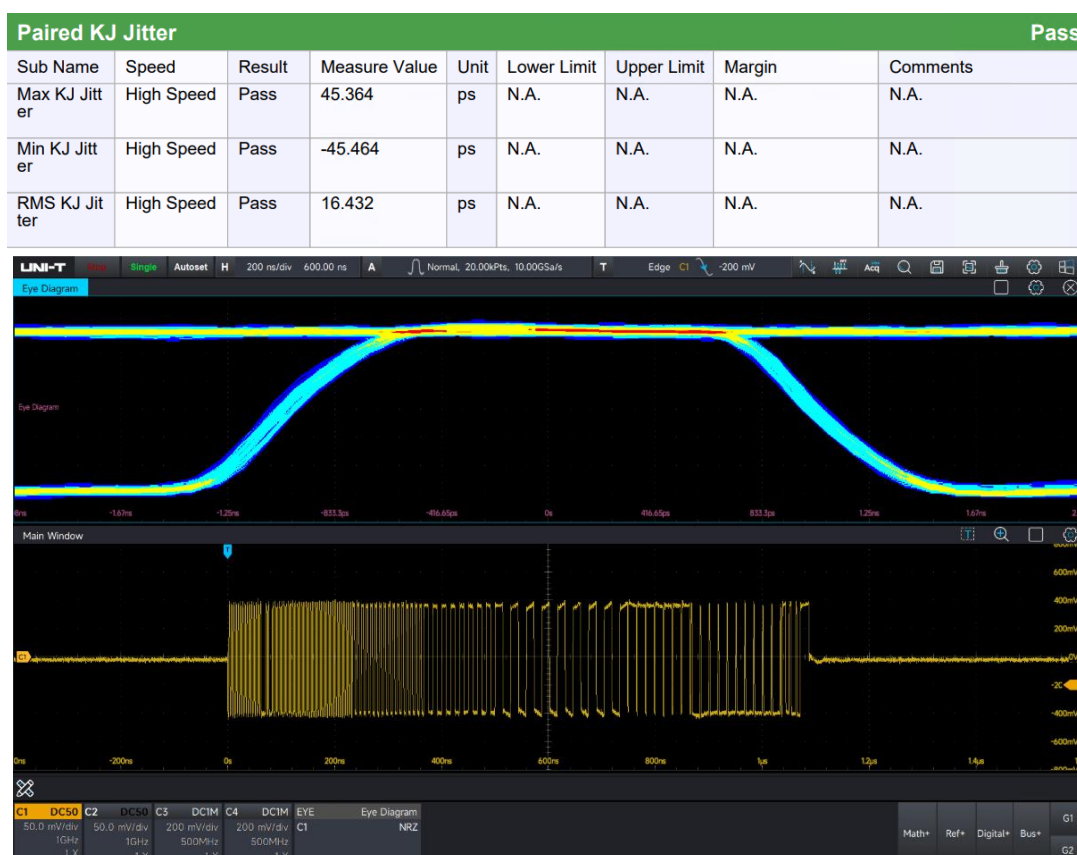
1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert a differential probe into the [D+ & D-] pins of the fixture [J6], and connect the other end to the oscilloscope according to the selected channel.

The diagram illustrates the setup for a "Device HS Upstream Signal Quality Test". It shows a laptop connected via a "USB Cable" to a "USB Device Test Fixture". The fixture has several ports: "DUT" (Device Under Test), "Differential probe" (connected to "D+" and "D-" pins), "USB-A" (connected to a "PC"), and "USB-B" (connected to a "Host Power"). A note at the bottom states: "Requires EDC or MIO controller".

Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.

- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.



KJ Pair Jitter Test Results

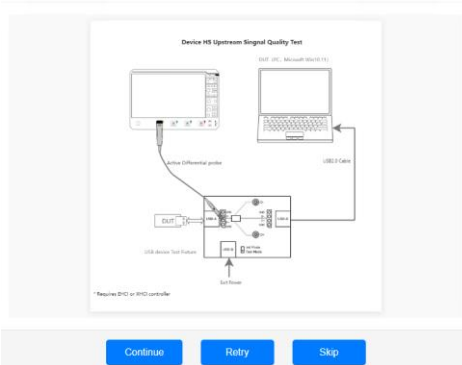
4.1.8 Edge Rise Rate

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Edge Rise Rate**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

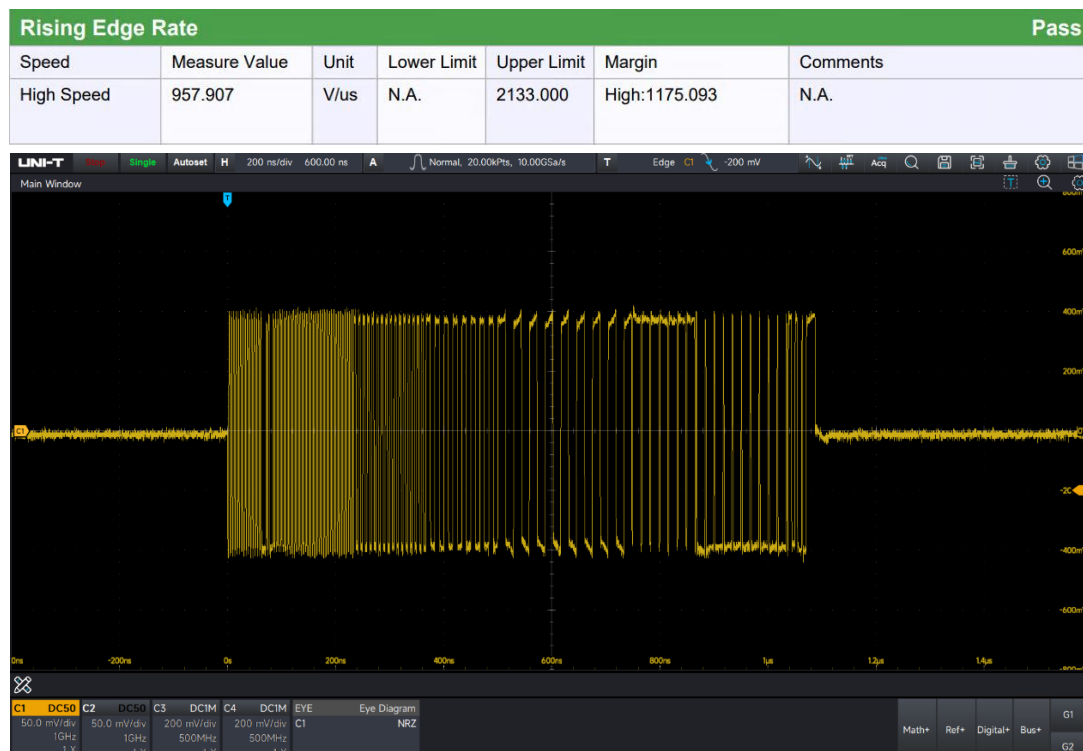
Device-HS-Rising Edge Rate

1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J3] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert a differential probe into the [D+ & D-] pins of the fixture [J6], and connect the other end to the oscilloscope according to the selected channel.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms. eform images.

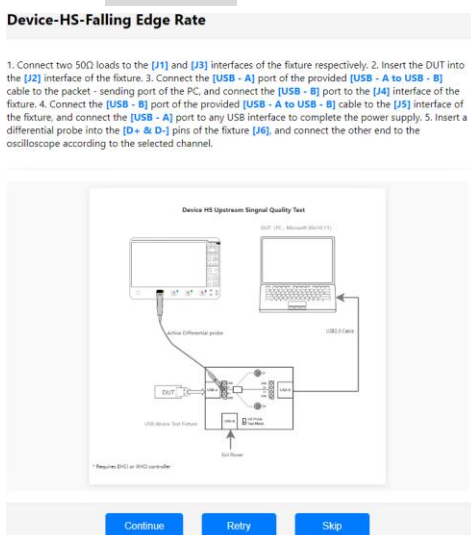


Edge Rise Rate Test Results

4.1.9 Edge Fall Rate

Test Procedure:

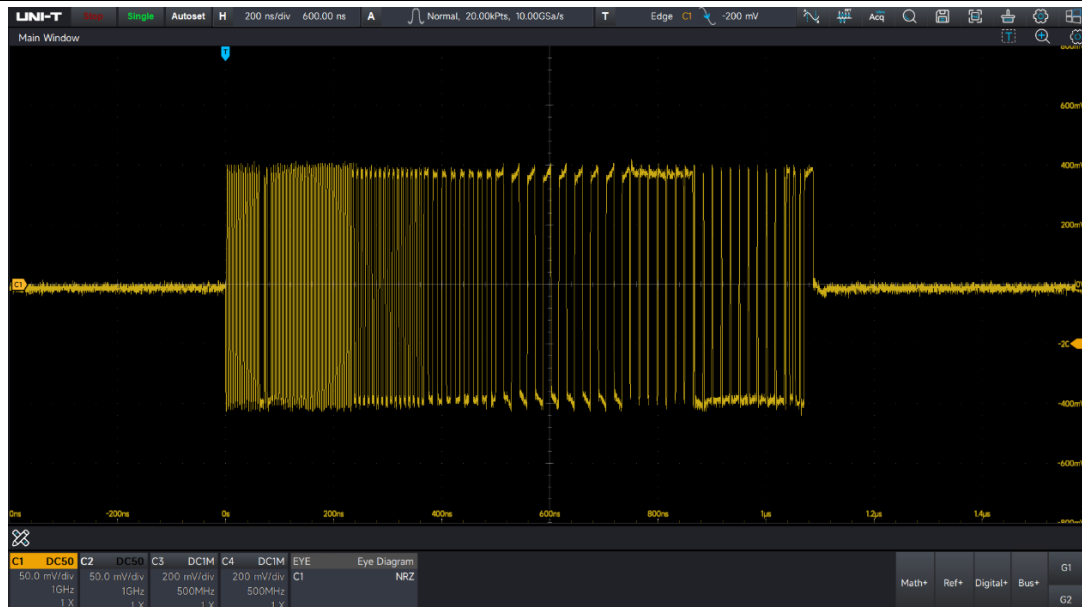
- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Edge Fall Rate**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.

Falling Edge Rate						Pass
Speed	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments
High Speed	954.053	V/us	N.A.	2133.000	High:1178.947	N.A.



Edge Fall Rate Test Results

4.1.10 Rise Time

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Rise Time**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

Device-HS-Rise Time

1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert a differential probe into the [D+ & D-] pins of the fixture [J6], and connect the other end to the oscilloscope according to the selected channel.

The diagram illustrates the setup for testing a USB device's upstream signal quality. It shows a PC connected to a USB Device Test Fixture via a USB Cable. The fixture is also connected to a DUT (Device Under Test) and an Oscilloscope. The fixture has multiple ports labeled J1 through J6. A note indicates that the test requires either a DUT or a PHY controller.

Device HS Upstream Signal Quality Test

DUT (PC, Microsoft Win10 x64)

OSCilloscope

USB Cable

Active Differential probe

J1 J2 J3 J4 J5 J6

USB Device Test Fixture

DUT

Oscilloscope

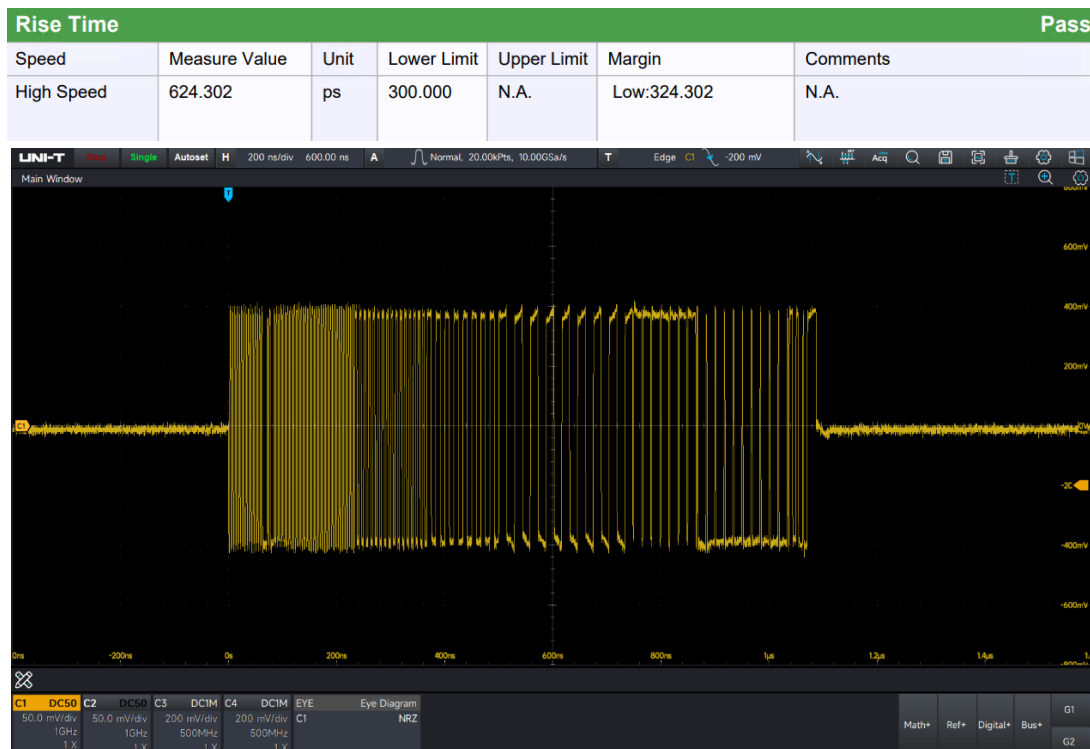
* Requires DUT or PHY controller

Continue Retry Skip

Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.

- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.



Rise Time Test Results

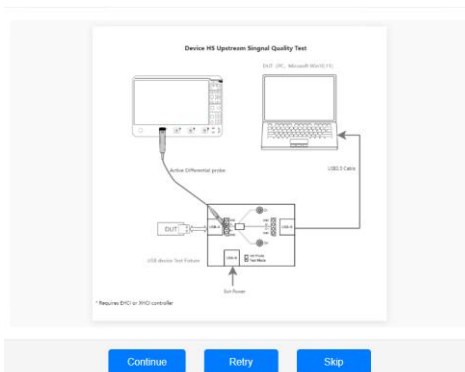
4.1.11 Fall Time

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Fall Time**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

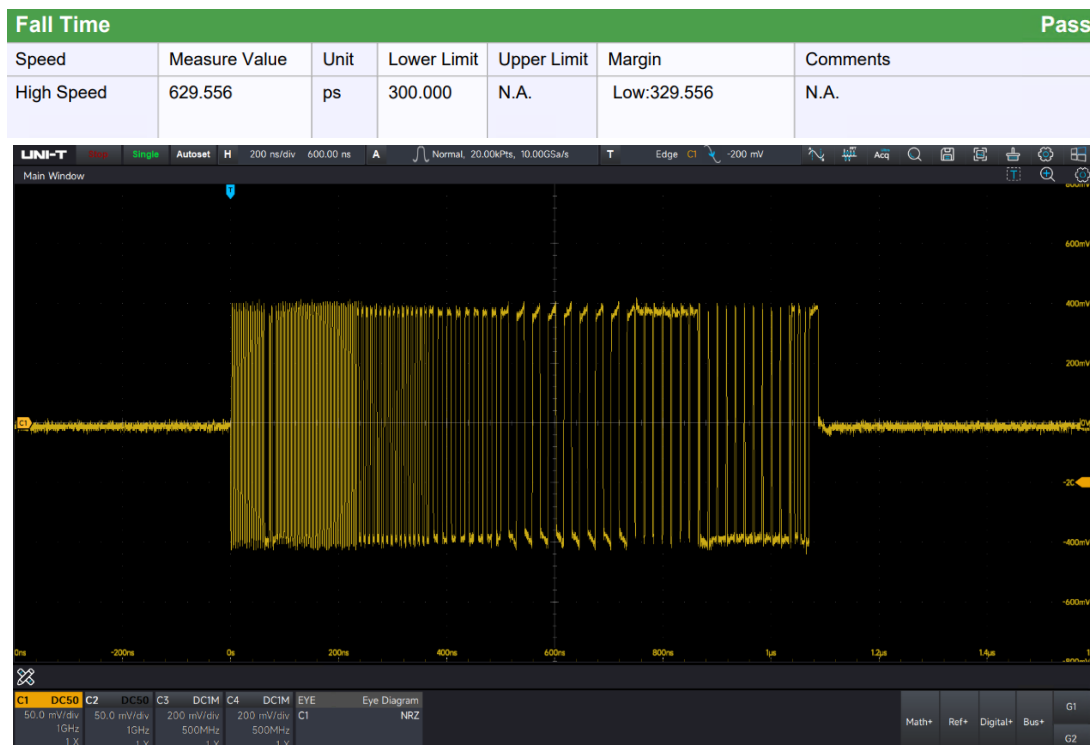
Device-HS-Fall Time

1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert a differential probe into the [D+ & D-] pins of the fixture [J6], and connect the other end to the oscilloscope according to the selected channel.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, click [Enumerate Bus], select the corresponding port, then click [Execute] to send the [TEST_PACKET] pattern. If the DUT is a Device, set the fixture switch to [TEST] mode.
- (7) Scope verifies test signals, configures acquisition, measures per compliance parameters, and records results. A report is generated with results and waveforms.



Fall Time Test Results

4.2 Non-Signal Quality Tests

4.2.1 Chirp Test

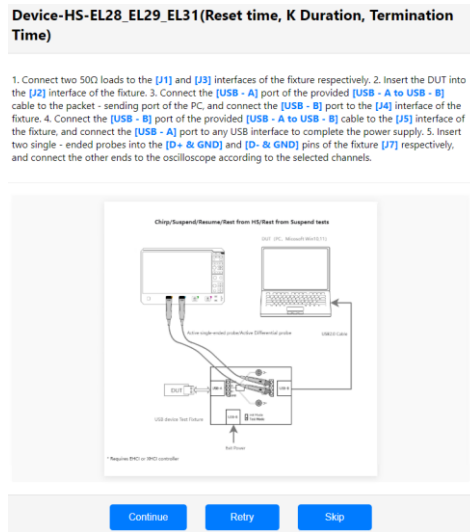
Chirp testing identifies high-speed devices during host-device high-speed negotiation. If negotiation fails, the device reverts to full-speed (12 Mbits). It checks basic timing and voltage of upstream and downstream ports in the speed detection protocol; hubs require testing on both ports.

When a device is hot-plugged, it enumerates immediately to capture the chirp handshake. During this, Chirp-K duration is measured to verify it's within 1.0 ms to 7.0 ms. After the K-J, K-J, K-J sequence, the device enables high-speed termination (amplitude drops from 800 mV to 400 mV). The time between the last J start in the sequence and termination activation must be $\leq 500 \mu\text{s}$. Chirp testing also measures the device's suspend/resume/reset timing and K/J amplitudes.

Test Procedure:

- (1) Open compliance software: **Test Setup** \rightarrow **Test Items**, click +, select **Chirp Test**.
- (2) In the **Waveform Acquisition** interface, under **Single-Ended**, select the corresponding analog channel.

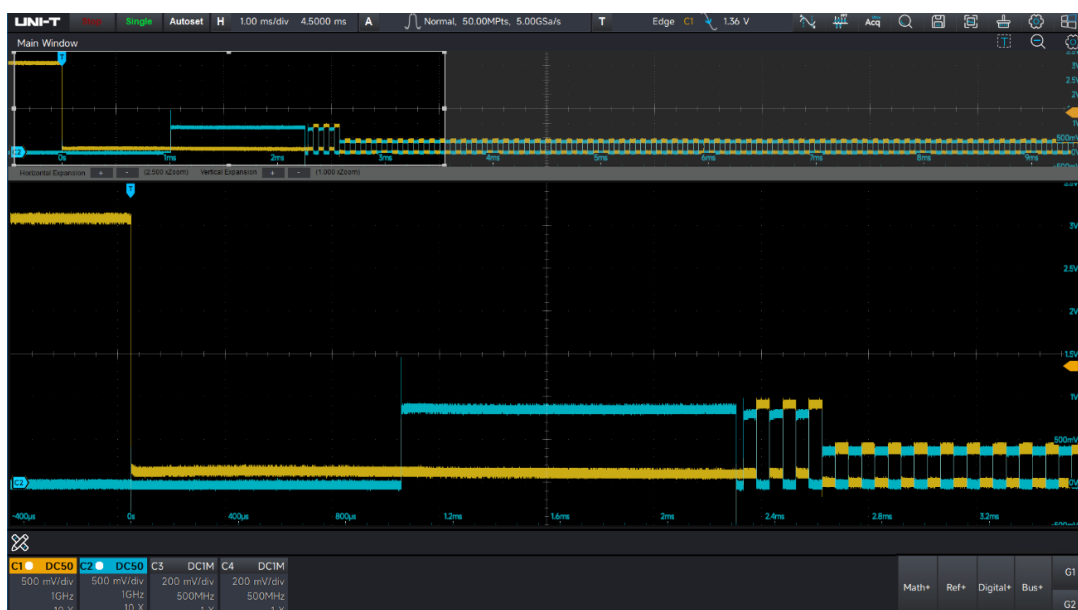
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, set the fixture switch to [INIT] mode, and click [Enumerate Bus].
- (7) Scope verifies test signals, configures acquisition, measures per compliance parameters, and records results. A report is generated with results and waveforms.

EL28_EL29_EL31(Reset time, K Duration, Termination Time)								Pass
Sub Name	Speed	Result	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments
EL28(Reset Time)	High Speed	Pass	1007.543	us	2.500	6000.000	High:4992.457 Low:1005.043	N.A.
EL29(K Duration)	High Speed	Pass	1.251	ms	1.000	7.000	High:5.749 Low:0.251	N.A.
EL31(Termination Time)	High Speed	Pass	0.327	us	N.A.	500.000	High:499.673	N.A.

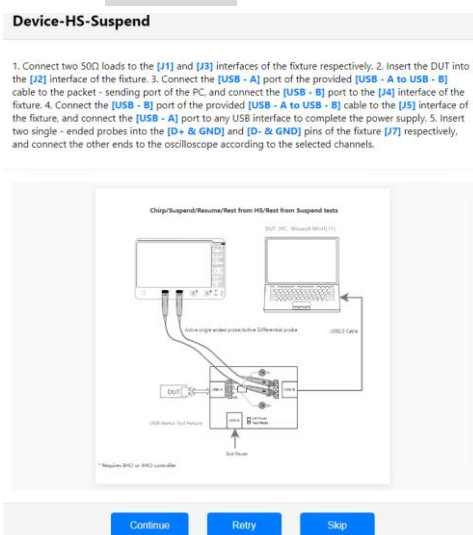


Chirp Test Results

4.2.2 Suspend Test

Test Procedure:

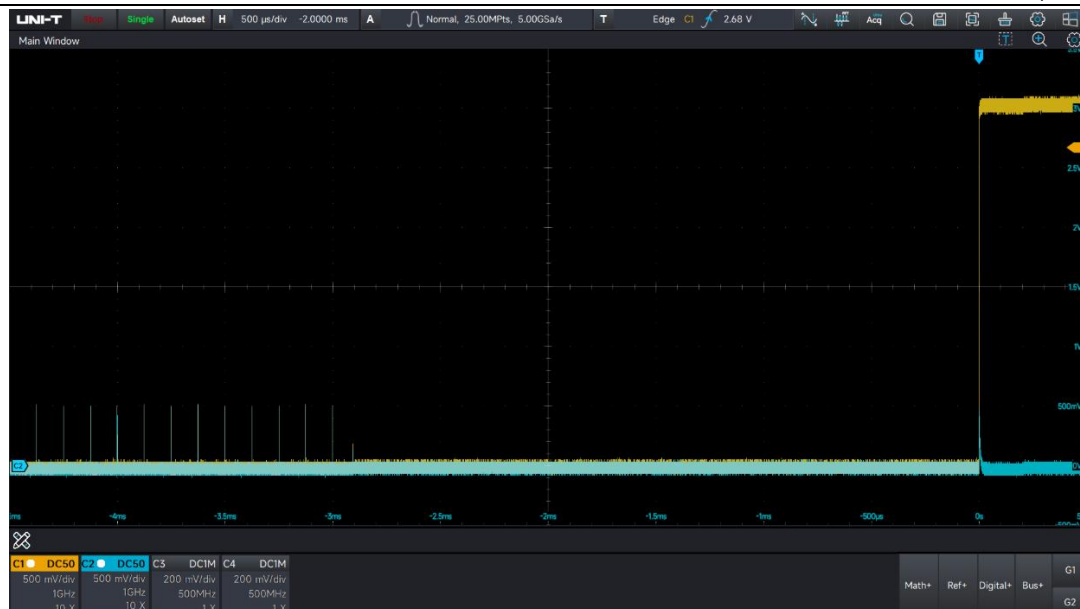
- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Suspend Test**.
- (2) In the **Waveform Acquisition** interface, under **Single-Ended**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts for packet software and fixture operation: Open [HSET] package tool, set fixture switch to [INIT] mode, click [Enumerate Bus].
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.

Suspend						Pass
Speed	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments
High Speed	3.000	ms	3.000	3.125	High:0.125 Low:0.000	N.A.



Suspend Test Results

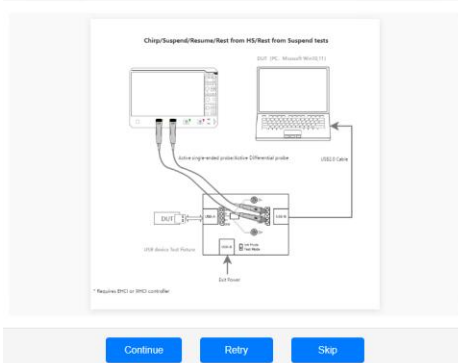
4.2.3 Resume Test

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Resume Test**.
- (2) In the **Waveform Acquisition** interface, under **Single-Ended**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

Device-HS-Resume

1. Connect two 500 loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert two single - ended probes into the [D+ & GND] and [D- & GND] pins of the fixture [J7] respectively, and connect the other ends to the oscilloscope according to the selected channels.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts: Open [HSETT], set fixture switch to [INIT] mode, click [Enumerate Bus], select port, choose [SUSPEND] mode and click [Execute], then choose [RESUME] and click [Execute].

- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.



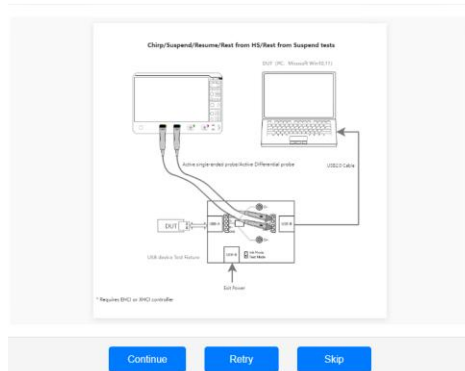
4.2.4 High-Speed Reset

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **High-Speed Reset**.
- (2) In the **Waveform Acquisition** interface, under **Single-Ended**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

Device-HS-Reset From HS

1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert two single - ended probes into the [D+ & GND] and [D- & GND] pins of the fixture [J7] respectively, and connect the other ends to the oscilloscope according to the selected channels.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts: Open [HSETT], set fixture switch to [INIT] mode, click [Enumerate Bus], select port, click [Execute], then choose [RESUME] and click [Execute].
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.



High-Speed Reset Test Results

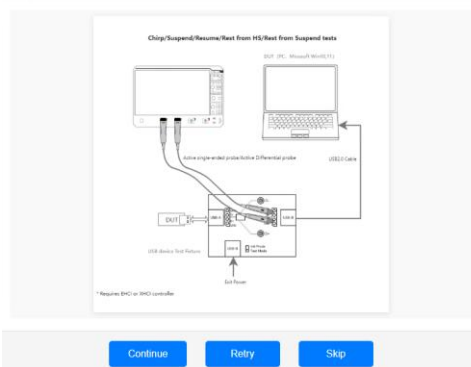
4.2.5 Suspend Reset

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Suspend Reset**.
- (2) In the **Waveform Acquisition** interface, under **Single-Ended**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

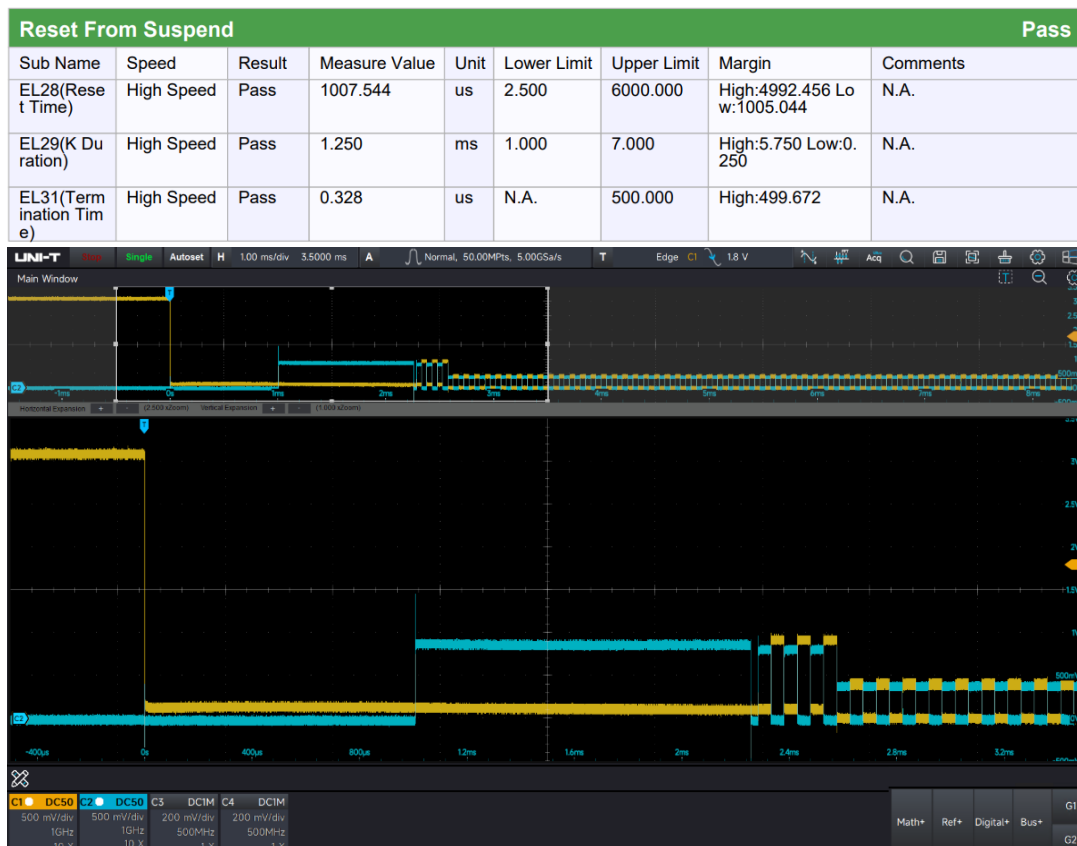
Device-HS-Reset From Suspend

1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert two single - ended probes into the [D+ & GND] and [D- & GND] pins of the fixture [J7] respectively, and connect the other ends to the oscilloscope according to the selected channels.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow prompts: Open [HSETT], set fixture switch to [INIT] mode, click [Enumerate Bus], select port, choose [SUSPEND] mode and click [Execute], then choose [RESUME] and click [Execute].
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms. eform images.

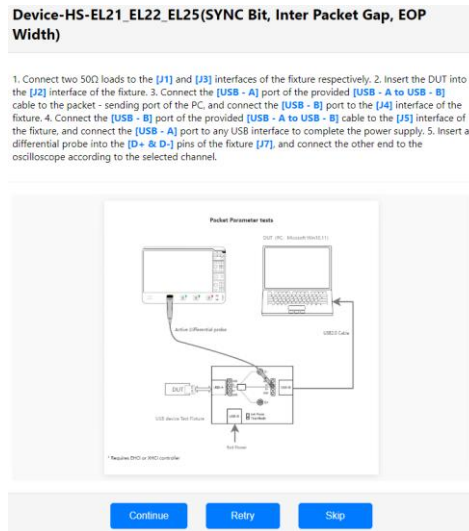


Suspend Reset Test Results

4.2.6 Packet Parameter Test

Test Procedure:

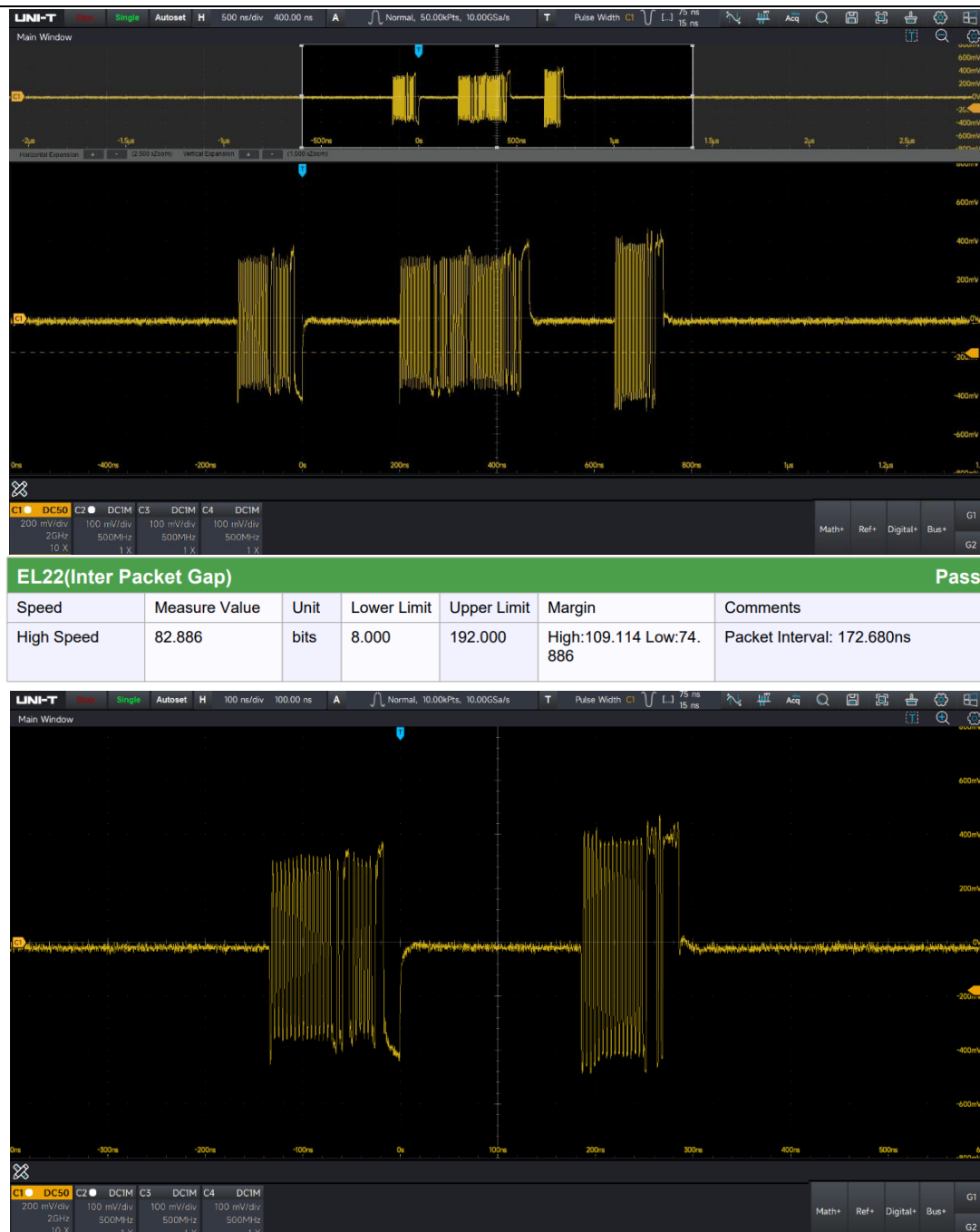
- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Packet Parameter Test**.
- (2) In the **Waveform Acquisition** interface, under **Differential**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow the software prompts to operate the packet tool and test fixture: Open [HSET], set the fixture to [INIT] mode, click [Enumerate Bus], select the target port, then click [Execute] to send [SINGLE STEP SET FEATURE] for Device DUT or [SINGLE STEP GET DEV DESC] for Host DUT.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms. eform images.

EL21_EL22_EL25(SYNC Bit, Inter Packet Gap, EOP Width)								Pass
Sub Name	Speed	Result	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments
EL21(SYN C Bit)	High Speed	Pass	32.071	bits	32.000	32.500	High:0.429 Low:0.071	SYNC Time: 66.814ns
EL22(Inter Packet Gap)	High Speed	Pass	83.281	bits	8.000	192.000	High:108.719 Low:75.281	Packet Interval: 173.502ns
EL25(EOP Width)	High Speed	Pass	7.896	bits	7.500	8.500	High:0.604 Low:0.396	EOP Interval: 16.451ns



Packet Parameter Test Results

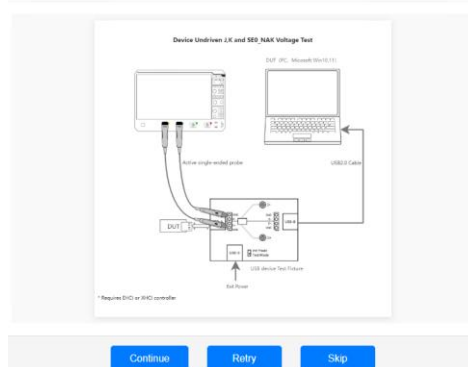
4.2.7 Undriven J/K Voltage Values, Voltage Value in SEO State

Test Procedure:

- (1) Open compliance software: **Test Setup** → **Test Items**, click +, select **Undriven J Voltage Value EL8 and Undriven K Voltage Value EL8**.
- (2) In the **Waveform Acquisition** interface, under **Single-Ended**, select the corresponding analog channel.
- (3) In the Limit Editor, set the test standard as needed, or leave at default Compliance standard.
- (4) Click **Start**.
- (5) Setup environment per diagram, click **Continue**.

Device-HS-Undriven J Voltage

1. Connect two 50Ω loads to the [J1] and [J3] interfaces of the fixture respectively. 2. Insert the DUT into the [J2] interface of the fixture. 3. Connect the [USB - A] port of the provided [USB - A to USB - B] cable to the packet - sending port of the PC, and connect the [USB - B] port to the [J4] interface of the fixture. 4. Connect the [USB - B] port of the provided [USB - A to USB - B] cable to the [J5] interface of the fixture, and connect the [USB - A] port to any USB interface to complete the power supply. 5. Insert two single - ended probes into the [D+ & GND] and [D- & GND] pins of the fixture [J6] respectively, and connect the other ends to the oscilloscope according to the selected channels.



Note: If a connection or waveform error occurs, the log will display a timeout and re-show the connection diagram. Follow the prompts to correct the connection, resend the waveform, and click **Continue** to proceed.

- (6) Follow the software prompts to operate the packet tool and test fixture: Open [HSET], click [Enumerate Bus], select the target port, then click [Execute] to send TEST_J pattern, set fixture switch to [TEST] mode.
- (7) Oscilloscope verifies test signals, configures acquisition, performs measurements according to compliance parameters, and records results. A report is generated with results and waveforms.eform images.

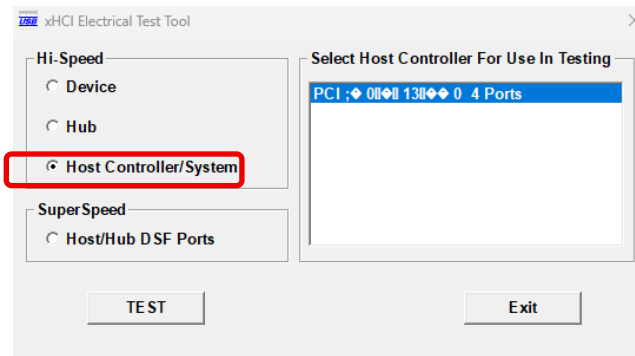
Undriven J Voltage							Pass	
Speed	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments		
High Speed	410.261	mV	360.000	440.000	High:29.739 Low:50.261	N.A.		
Undriven K Voltage							Pass	
Speed	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments		
High Speed	406.268	mV	360.000	440.000	High:33.732 Low:46.268	N.A.		
Undriven SE0_NAK Voltage							Pass	
Sub Name	Speed	Result	Measure Value	Unit	Lower Limit	Upper Limit	Margin	Comments
D+ Voltage	High Speed	Pass	4.957	mV	-20.000	20.000	High:15.043 Low:24.957	N.A.
D- Voltage	High Speed	Pass	2.441	mV	-20.000	20.000	High:17.559 Low:22.441	N.A.



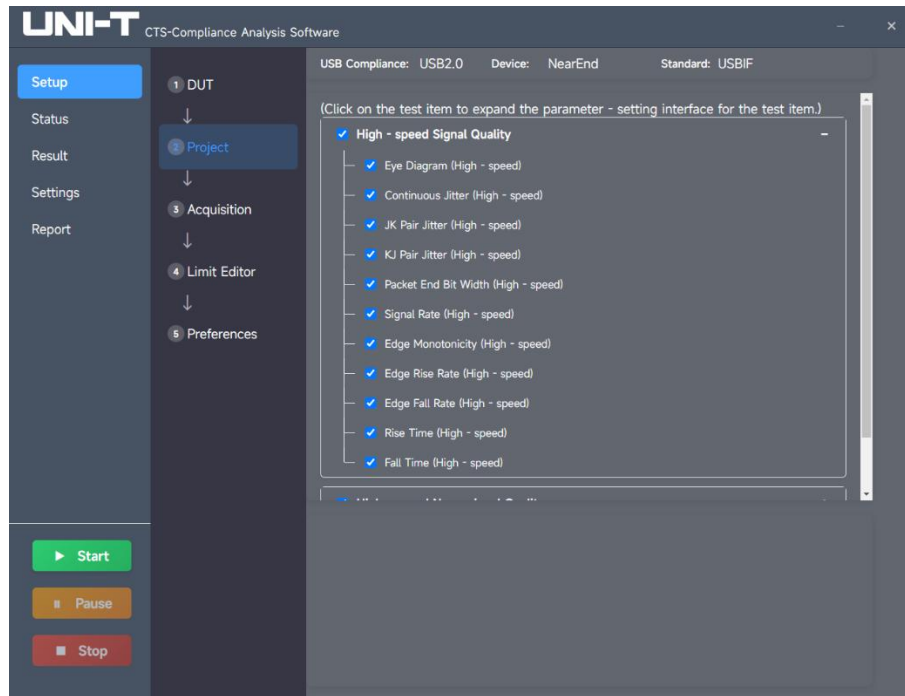
Notes:

1. Signal/non-signal quality test items differ between Device and Host. Strictly follow the compliance software's guidance for cabling, packet software, and fixture operation to ensure test validity. This example demonstrates Device high-speed signal/non-signal quality tests. For Host testing, select Host

as the test object in the packet software and follow the TEST prompts.



2. These examples show single-item testing. For multi-item testing, simply select the required test items, configure the probe type, and click Start.



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